What is claimed is:

1. A semiconductor device comprising:

a cell array region formed in a semiconductor substrate and including a capacitor having a lower electrode, the lower electrode having a lower electrode heght;

a peripheral circuit region formed in the semiconductor substrate and including a first metal wiring, the first metal wiring having a first metal thickness;

a first insulating layer formed on the cell array region and the peripheral circuit region and having openings in which the lower electrode is formed; and

a second insulating layer formed on the first insulating layer, the first metal wiring being arranged in the second insulating layer,

wherein the lower electrode height and the first metal thickness are substantially identical, and wherein a lower surface of the lower electrode and a lower surface of the first metal wiring are in a substantially planar orientation.

2. The semiconductor device of claim 1, further comprising:

a first conductive plug extending through the first insulating layer to connect the lower electrode to the semiconductor substrate; and

a second conductive plug extending through the first insulating layer to connect the first metal wiring to the semiconductor substrate.

3. The semiconductor device of claim 2, further comprising a conductive landing structure arranged in the second insulating layer and having a pad thickness, wherein the pad thickness is substantially identical to the first metal thickness, and wherein a lower surface of the landing structure and the lower surface of the first metal wiring are in a planar orientation.

4. The semiconductor device of claim 3, further comprising a third conductive plug extending through the first insulating layer to connect the landing structure to the semiconductor substrate.

5. The semiconductor device of claim 1, further comprising:

first gate structures formed in the cell array region, the first insulating layer being formed on the first gate structures;

second gate structures formed in the peripheral region, the first insulating layer being formed on the second gate structures;

a first storage node contact hole and a first bit line contact hole formed through the first insulating layer for exposing a first surface of the substrate in the cell array region;

first metal contact holes formed through the first insulating layer for exposing the first and second gate structures and a second surface of the substrate in the peripheral region;

conductive plugs formed in the first storage node contact hole, the first bit line contact hole and the first metal contact hole, the first metal wiring being in

electrical contact with the conductive plug in the first metal contact hole;

a capacitor formed in the second insulating layer in the cell array region, the capacitor being in electrical contact with the conductive plug in the first storage node contact hole;

an insulating interlayer formed on the capacitor, the first metal wiring and the second insulating layer; and

a second metal wiring formed on the insulating interlayer in the peripheral region, the second metal wiring being electrically connected to the first metal wiring.

6. The semiconductor device of claim 5, wherein the peripheral region includes at least one of core circuitry, peripheral circuitry and logic circuitry.

7. The semiconductor device of claim 5, wherein the capacitor has a metal/insulator/metal structure.

8. The semiconductor device of claim 5, further comprising a bit line formed on the insulating interlayer and electrically connected to the conductive plug in the first bit line contact hole through a second bit line contact hole formed through the insulating interlayer, wherein the bit line and the second metal wiring are formed from a single metal layer.

9. The semiconductor device of claim 5, wherein the insulating interlayer includes a first sublayer formed on the first metal wiring and a second sublayer formed on the capacitor, the first metal wiring and the first sublayer.

10. The semiconductor device of claim 4, wherein the landing structure has a pad width W_{LP} and the third conductive plug has a plug width W_{CP}, wherein the relationship $W_{LP}>W_{CP}$ is satisfied.

11. A method for manufacturing a semiconductor device comprising:

providing a semiconductor substrate having a cell array region and a peripheral region;

forming a first insulating layer on the semiconductor substrate;

forming a second insulating layer on the first insulating layer;

forming a first metal wiring having a first metal thickness in the second insulating layer in the peripheral region; and

forming a capacitor having a lower electrode in the second insulating layer in the cell array region, the lower electrode having a lower electrode height,

wherein the first metal thickness and the lower electrode height are substantially identical, and wherein a lower surface of the first metal wiring and a lower surface of the lower electrode are in a substantially planar orientation.

12. The method of claim 11, wherein forming the first metal wiring

comprises:

forming a first metal layer on the first insulating layer;

patterning the first metal layer to form the first metal wiring;

forming the second insulating layer on the first metal wiring; and

removing an upper portion of the second insulating layer to expose an upper surface of the first metal wiring.

13. The method of claim 11, wherein forming the first metal wiring comprises;

forming a second insulating layer on the first insulating layer;

patterning the second insulating layer to form first metal wiring openings, the first metal wiring openings extending to an upper surface of the first insulating layer;

forming a first metal layer on the second insulating layer and the first metal wiring openings, the first metal layer having a thickness sufficient to fill the first metal wiring openings; and

removing an upper portion of the first metal layer to expose an upper surface of the second insulating layer and form the first metal wiring.

14. The method of claim 11, wherein forming the first metal wiring comprises forming a landing structure in the second insulating layer in the cell array region, the landing structure having a pad thickness, wherein the first metal

thickness and the pad thickness are substantially equal and wherein a lower surface of the first metal wiring and a lower surface of the landing structure are in a substantially planar orientation.

15. The method of claim 14, wherein forming the landing structure further comprises:

forming a first metal layer on the first insulating layer;

patterning the first metal layer to form the first metal wiring and the landing structure;

forming the second insulating layer on the first metal wiring and the landing structure; and

removing an upper portion of the second insulating layer to expose an upper surface of the first metal wiring and an upper surface of the landing structure.

16. The method of claim 14, wherein forming the landing structure further comprises:

forming a second insulating layer on the first insulating layer;

patterning the second insulating layer to form first metal wiring openings and a landing structure opening, the first metal wiring openings and the landing structure opening extending to an upper surface of the first insulating layer;

forming a first metal layer on the second insulating layer, the first metal

layer having a thickness sufficient to fill the first metal wiring openings and the landing structure opening; and

removing an upper portion of the first metal layer to expose an upper surface of the second insulating layer to form the first metal wiring and the landing structure.

17. The method of claim 11, further comprising:

forming first gate structures in the cell array region;

forming second gate structures in the peripheral region;

forming the first insulating layer on the substrate having the first and second gate structures;

etching the first insulating layer to form a first storage node contact hole and a first bit line contact hole for exposing a first surface of the substrate in the cell array region, and first metal contact holes for exposing the first and second gate structures and a second surface of the substrate in the peripheral region;

forming conductive plugs in the first storage node contact hole, the first bit line contact hole and the first metal contact hole;

forming a second insulating layer on the first insulating layer and the conductive plugs;

forming a first metal wiring in the second insulating layer in the peripheral region, the first metal wiring being in electrical contact with the conductive plug in the metal contact hole; and

forming a capacitor in the second insulating layer in the cell array region, the capacitor being in electrical contact with the conductive plug in the storage node contact hole.

18. The method of claim 17, further comprising:

forming an insulating interlayer on the capacitor, the first metal wiring and the second insulating layer;

forming a second metal contact hole in the insulating interlayer; and

forming a second metal wiring to electrically make contact with the first metal wiring through the second metal contact hole.

19. The method of claim 18, further comprising:

forming a second bit line contact hole through the insulating interlayer during the formation of the second metal contact hole, the second bit line exposing an upper surface of the conductive plug in the first bit line contact hole; and

forming a bit line during the formation of the second metal wiring, the bit line being in electrical contact with the conductive plug in the first bit line contact hole.

20. The method of claim 17, further comprising:

after forming the first metal wring, forming a first insulating sublayer on the first metal wiring and the second insulating layer in the cell array region;

forming a capacitor opening that extends through the first insulating sublayer and exposed an upper surface of the conductive plug in the storage node contact hole;

forming the capacitor in the capacitor opening; and

forming a second insulating sublayer on the capacitor and the first insulating sublayer, the first and second insulating sublayers cooperating to form the insulating interlayer.

21. The method of claim 20, further comprising planarizing the first insulating sublayer before forming the capacitor opening.

22. A method of fabricating a semiconductor device comprising:

providing a semiconductor substrate having a cell array regions and a peripheral regions;

forming first gate structures in the cell array region;

forming second gate structures in the peripheral region;

forming a first insulting layer on the first and second gate structures;

forming a storage node contact hole and a bit line contact hole through the first insulating layer, thereby exposing a first surface of the substrate in the cell array region;

forming metal contact holes through the first insulating layer, thereby exposing the first and second gate structures and a second surface of the substrate

in the peripheral region;

forming conductive plugs in the storage node contact hole, the bit line contact hole and the metal contact holes;

forming a second insulating layer on the first insulating layer and the conductive plugs;

forming the first metal wiring in the second insulating layer, the first metal wiring being in electrical contact with the conductive plug in the metal contact hole;

forming a capacitor in the second insulating layer, the capacitor being in electrical contact with the conductive plug in the storage node contact hole;

forming an insulating interlayer on the capacitor, the first metal wiring and the second insulating layer; and

forming a second metal wiring on the insulating interlayer, the second metal wiring being electrically connected to the first metal wiring.